What is claimed is:

1. A method of converting code to a hardware realization, the method comprising steps of:
receiving user code including at least one algorithm specification, at least one data representation specification, and at least one data communication specification; and
compiling the user code, wherein the user code is used to create a digital circuit.

2. The method of claim 1, wherein the step of compiling further comprises steps of:
compiling the user code to generate a netlist; and
mapping the netlist using physical design tools for creating the digital circuit.

3. The method of claim 1, further comprising a step of creating the digital circuit based on the user code.

4. The method of claim 3, wherein the step of creating further comprises steps of:
creating configuration data; and
subsequently configuring an FPGA.

5. The method of claim 3, wherein the step of creating further comprises creating a specification for one of a custom-designed VLSI chip and a standard cell VLSI chip.

6. The method of claim 1, wherein the step of compiling further comprises retrieving information from libraries, the information being associated with the at least one algorithm specification, the at least one data representation specification, and the at least one data communication specification.

7. The method of claim 1, wherein the at least one algorithm specification includes at least one variable having a defined set of values not varying by platform and at least one operator having a function not varying by platform.

8. The method of claim 1, wherein the at least one data representation specification includes one of 2's-complement, signed-digit, and fully-redundant carry-save for each variable in the at least one algorithm specification.

9. The method of claim 1, wherein the at least one data communication specification includes one of bit-serial, digit-serial and fully-parallel for each variable in the at least one algorithm specification.

10. The method of claim 1, wherein the step of receiving the user code further comprising receiving selections of the at least one algorithm specification, the at least one data representation specification, and the at least one data communication specification from a graphical user interface (GUI).

11. The method of claim 1, wherein the at least one algorithm specification, the at least one data representation specification, and the at least one data communication specification are independent and each of these specifications are modifiable without affecting the others.

12. A method of converting code to a hardware realization, the method comprising steps of:

receiving user code;

identifying variables used in an operation in the user code, the operation including at least one operator;

identifying a set of assumable values for each of the identified variables;

calculating a set of assumable values for other variables holding the results of the operation based on the identified set of assumable values; and

compiling the user code, wherein the user code is used to create a digital circuit.

13. The method of claim 12, wherein the user code further includes at least one algorithm specification, at least one data representation specification, and at least one data communication specification.

14. The method of claim 13, wherein the at least one data representation specification includes one of 2's-complement, signed-digit, and fully-redundant carry-save for each variable in the at least one algorithm specification.

15. The method of claim 13, wherein the at least one algorithm specification, the at least one data representation specification, and the at least one data communication specification are independent, such that each of these specifications are modifiable without affecting the others.

16. A system operable to create a digital circuit, the system comprises:

a compiler compiling user code, the user code including at least one algorithm specification, at least one data representation specification, and at least one data communication specification; and

a digital circuit created from the compiled user code.

17. The system of claim 16, further comprising a plurality of libraries connected to the compiler, the plurality of libraries including information associated with the at least one algorithm specification, the at least one data representation specification, and the at least one data communication specification, wherein the compiler retrieves the information to compile the user code.

18. The system of claim 16, wherein the compiler compiles the user code to generate a netlist that lists components in the digital circuit.

19. The system of claim 18, further comprising physical design tools, the physical design tools being used to create the digital circuit from the netlist.

20. The system of claim 16, wherein the at least one algorithm specification includes variables and an operator in an operation in the user code, and each of the variables includes an identifiable set of assumable values to be used in the operation.

21. The system of claim 20, wherein the compiler is operable to calculate a set of assumable values for a variable in the operation performed by an operator holding a result of the operation based on the identified set of assumable values for the variables used in the operation.